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Molecular Electronics with Carbon Nanotubes

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ABSTRACT
Carbon nanotubes have unique properties that make them a most promising system on which to base molecular electronics. We briefly review the electrical characteristics of carbon nanotubes, and then focus on carbon nanotube field-effect transistors (CNTFETs). Procedures by which hole-transport, electron-transport and ambipolar CNTFETs can be fabricated are presented, and their electrical characteristics are discussed and compared with those of Si MOSFETs. Ways to fabricate arrays of CNTFETs are also demonstrated, and electron and hole CNTFETs are integrated to form complementary logic circuits.

Introduction

We are all well aware of the extraordinary advances in silicon-based electronic technology over the past several decades. In the integrated circuit era, this progress has been achieved primarily through the scaling of the metal-oxide-semiconductor field-effect transistor (MOSFET) into smaller and smaller dimensions, thereby leading to both higher speed and device density.[1] However, it is now generally accepted that silicon devices will be reaching some fundamental scaling limits in a decade or so. This realization has sparked an intense search for alternative technologies, an effort that involves searching for both new device principles and materials. In this search, scientists are guided by the experience gained during decades of device research and by the performance standards set by the highly advanced silicon technology. At IBM, we are interested in logic systems, in which devices are always part of a large and complex system. It is crucial, therefore, that any future devices exhibit amplification so that signals can be referenced and restored to a reference voltage at each stage of a long chain of logical operations.[2] Logical systems built without it would be susceptible to noise from thermal fluctuations and external environmental disturbances as well as signal variations arising from the unavoidable manufacturing variations and aging of the devices themselves. For these reasons, we have concentrated our efforts on three-terminal nanotransistors, specifically, on field-effect transistors that have been proven to be the most useful form of transistor.[2]

Phaedon Avouris received his B.S. degree from the Aristotelian University in Greece and his Ph.D. in physical chemistry from Michigan State University in 1974. After postdoctoral work at UCLA and AT&T Bell Laboratories, he joined IBM's Research Division in 1978. Currently, he is manager of Nanoscale Science and Technology at the IBM T. J. Watson Research Center. His research interests include molecular and nanoelectronics, low-dimensional systems, and surface chemistry and physics.

One promising direction for the transistors of the future involves "molecular electronics" in which the active part of the device is composed of a single or a few molecules.[3] The most widely studied forms of molecular electronics is based on carbon nanotubes.[4,5] Carbon nanotubes (CNTs) are macromolecular systems with unique physical and chemical properties.[6] Depending on their chirality, they can be metals or semiconductors. The small diameter and long length of single-walled carbon nanotubes (SWCNTs) lead to very large aspect ratios that make them almost ideal one-dimensional (1D) systems. This in turn implies drastically reduced carrier scattering and the possibility of ballistic devices. Furthermore, in CNTs, all chemical bonds are satisfied and very strong, leading to extremely high mechanical, thermal, and chemical stability. The lack of interface states as in the silicon/silicon dioxide interface provides a greater flexibility to the fabrication process.

The Electronic Structure and Electrical Properties of Carbon Nanotubes

The electronic structure and electrical properties of SWCNTs can be deduced from those of a layer of graphite ("graphene sheet").[4,5,7,8] A CNT can be thought of as being formed by rolling a piece of graphene to create a seamless cylinder (see Figure 1A). The intriguing electrical properties of CNTs are due, to a large part, to the peculiar electronic structure of graphene. Its band structure and the hexagonal shape of its first Brillouin zone are shown in Figure 1B. The valence π and conduction π^* states are seen to join at six points lying at the Fermi energy (Fermi points). In most directions in k-space, as in the Γ-M direction, the electrons encounter a semiconductor-like band gap. In the Γ-K direction and in five other directions that pass through the Fermi points, or K-points, the electrons have free motion, and the graphene behaves as a metal.

In CNTs, we need to take into account the confinement of the electrons around the circumference of the CNT. This is accomplished by introducing a new quantization condition, namely, $k_C C = 2\pi j$, where k_C is the wavevector in the circumferential direction; C, the chirality vector; and j, an integer. Thus, each band of graphene (σ, σ^*, π, π^*) splits into a number of one-dimensional (1D) subbands labeled by j. Figure 1B shows the states of a (3,3) CNT. The allowed energy states j of the tube are cuts (indicated by the black lines) of the graphene band-structure. In the case of the (3,3) tube, two of these cuts pass through the K Fermi point, and the tube is metallic. In cases in which no cut passes through a K-point, the tube is semiconducting. It can be shown that (n,m) tubes are metallic when $n = m$; tubes with $n - m = 3i$, where i is an integer, have a small curvature-induced band-gap; and CNTs with $n - m \neq 3i$ are semiconducting.[4,5,7−9]

In semiconducting CNTs (s-CNTs) the subbands do not cross at E_F, but a band-gap $E_{GAP} = (4\hbar v_F/3dv_{CNT})$, where

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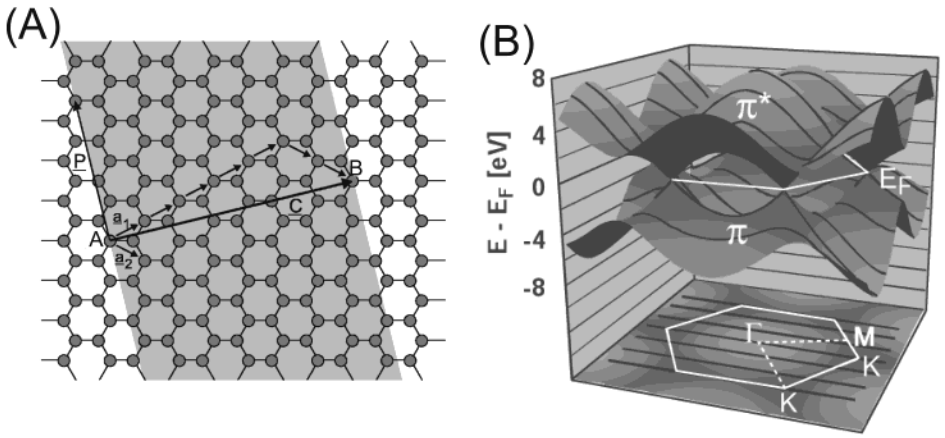

FIGURE 1. (A) Generation of a carbon nanotube (CNT) by folding a section of a graphene sheet. The folding and the resulting nanotube are characterized by the chirality vector $C = na_1 + ma_2 \equiv (n,m)$, where a_1 and a_2 are the unit vectors of the hexagonal lattice. When point B is brought over point A, a tube with a circumference C is generated. In the example shown here, $C = 5a_1+2a_2$, and the tube is labeled as (5,2). (B) Top: Band-structure of the 2D graphene sheet (gray surface). The valence and conduction bands meet at six points (K-points) lying at the Fermi energy. Bottom: The first Brillouin zone of graphene. The black lines represent the allowed states of a (3,3) nanotube. They are cuts of the graphene bandstructure that are selected by imposing the condition that the perpendicular wavevector k_C satisfies the quantization condition: $k_C C = 2\pi j$, where j is an integer. If the states pass through a K-point (as in this case) the tube is a metal, but if they do not, the tube is a semiconductor.

d_{CNT} is the tube's diameter and v_F is the Fermi velocity, is present.[4,5,7,8] The above theoretical predictions have been confirmed experimentally by STS.[9−11]

The unique electrical properties of SWCNTs arise from the confinement of the electrons in CNTs, which allows motion in only two directions along the tube axis: forward and backward, along with the requirements for energy and momentum conservation. These three constraints lead to a reduced "phase space" for the scattering processes that are responsible for the electrical resistance of the m-CNTs.[4,5,12] Because of the reduced scattering, m-CNTs can carry enormous current densities up to 10^9A/cm^2 without being destroyed.[13] This density is about 2−3 orders of magnitude higher than is possible in metals such as Al or Cu.

In the absence of any scattering, when transport is ballistic, the two-terminal conductance of a 1D system is given by Landauer's equation,[14] $G = (2e^2/h)\sum_i^N T_i$, where $2e^2/h$ is the quantum of conductance, and T_i is the transmission of each contributing subband (conduction channel) produced by the confinement of the electrons along the circumference of the CNT. In the absence of scatttering ($T_i = 1$), the resistance ($R = 1/G$) at low electron energies of a m-SWCNT is given by Landauer's equation with $N = 2$ (two subbands crossing at E_F) is ∼6.5 kΩ. This resistance is a contact resistance arising from the mismatch of the number of conduction channels in the CNT and the macroscopic metal leads.[15] In addition to this quantum mechanical contact resistance, there are other sources of contact resistance, such as that produced by poor coupling between the CNT and the leads, or Schottky barriers at metal/semiconducting-CNT junctions.[16] These types of resistances are very important and can dominate and obscure the intrinsic electrical properties of CNTs.

To measure the electrical properties of individual CNTs, we have to connect them with the external macroscopic world. For this purpose, the nanotube is connected to metal electrodes produced by lithographic techniques (see Figure 2). Wire bonding of the device takes place at the large square pads at the top left image.

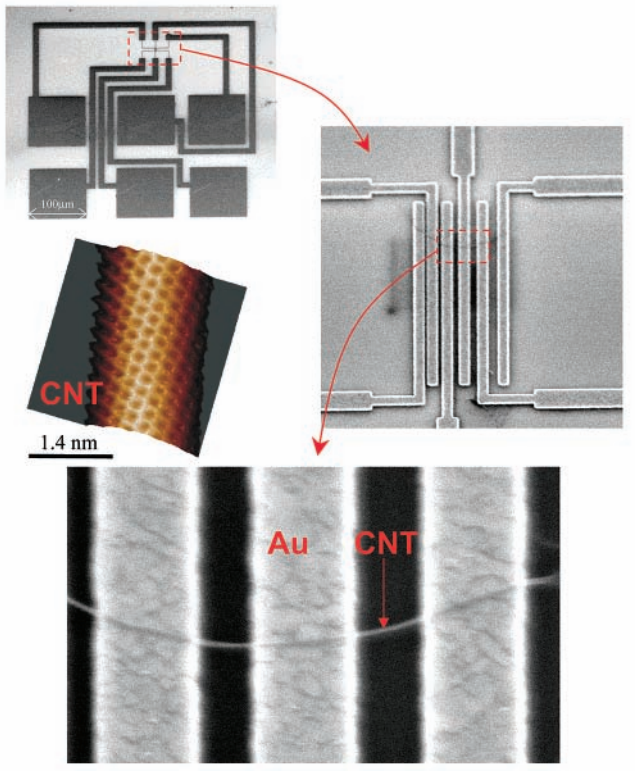

FIGURE 2. Electron microscope image of the metal electrodes used to measure the electrical properties of individual CNTs. The inset shows an atomic resolution scanning tunneling microscope (STM) image of a CNT.

Field-Effect Transistors

Before we discuss the work on CNTFETs, we review some of the basic concepts involved. For simplicity, we use a

classical description of the electrical transport process in the transistor. We expect, however, that even in the case of quantum transport, this treatment can provide a helpful phenomenological description.[17]

The basic FET structure involves two metal electrodes designated as "source" and "drain" connected by a semiconducting channel. In conventional devices, the channel is made of Si; however, in CNTFETs, the channel is replaced by a s-CNT. A third electrode, the "gate," is separated from the channel by a thin insulator film. Normally, if no charge is placed on the gate, no charge flows into the channel. In a p-type (i.e., hole conducting) FET, when a negative charge is placed on the gate and the applied voltage V_{GS} exceeds a certain threshold, V_{Th}, then a hole current flows through it. Similarly, for an n-type FET, an electron current flows when a positive charge is on the gate and the voltage exceeds the threshold.

To develop a quantitative account of the switching process, we need to know the detailed transport mechanism of the carriers in the channel of the FET. Whereas in m-SWCNTs, transport is ballistic (i.e., there is no scattering over length scales of the order of many hundreds of nanometers or even micrometers), transport in s-SWCNTs is more complicated. Scattering by short-ranged potentials is more efficient in semiconducting tubes,[18] and electrons with sufficient energy can excite optical phonons.[19] Furthermore, the energy states of s-CNTs are much closer in energy than in m-CNTs, and interband scattering may become important.[20] Experiments suggest that in this case, transport is diffusive-like,[18,21] and the carriers in the channel move with a drift velocity $v = \mu\mathcal{E}$, where μ is the effective carrier mobility, and $\mathcal{E}$, the electric field. The amount of charge Q_C that flows through the nanotube channel is: $Q_C = C_G(V_{GS} - V_{Th})$, where C_G is the gate capacitance. The source-drain current ($I_{DS} = Q_C$/transit time) is then given by eq 1,

$$I_{DS} = \mu\mathcal{E}C_G(V_{GS} - V_{Th})/L \qquad (1)$$

where L is the channel length. When the gate−channel capacitor is a simple parallel plate type, as in silicon FETs, then, $C_G = \epsilon A/t_{OX}$, where A is the plate area, ϵ is the dielectric constant, t_{OX} is the gate oxide thickness, and $\mathcal{E} = V_{DS}/L$.

From eq 1, which is valid for $V_{DS} < (V_{GS} - V_{Th})$, we see that the current in the channel is proportional to this voltage. Therefore, the FET can be viewed as a variable resistor with a resistance controlled by the gate voltage, V_{GS}. At high V_{DS}, current saturation results as a result of channel pinch-off or carrier velocity saturation.[1,17] An important characteristic of an FET is its transconductance, g_m ($\equiv |dI_{DS}/dV_{GS}|_{VDS} =$ constant), a measure of the switching speed of the device.

Because the FET has to be able to drive other devices down the line, it is important to optimize its current drive. According to eq 1, I_{DS} and g_m can be increased by increasing the gate capacitance C_G and the carrier mobility or by decreasing the length of the channel. In a CNTFET, however, C_G will not be that of a parallel plate capacitor, as in Si. A better approximation is provided by the capacitance of a wire (nanotube) at a distance h over a conducting plane (gate); i.e., $C_G = 2\pi L\epsilon\epsilon_0/\ln(2h/r)$, where r and L are the nanotube radius and length, respectively, and $h = t_{OX} + r$.[21] The behavior is qualitatively the same as in a planar Si device; however, in a CNTFET, I_{DS} would increase more slowly with decreasing t_{OX}.

In the above discussion, we used a phenomenological approach based on diffusive-like transport in a long nanotube comprising the channel of the FET. Such a transport mechanism is expected to apply to long s-CNTs. In short, undamaged tubes at low bias, transport can be ballistic. In this case, the carriers move without scattering inside the tube with a velocity close to the Fermi velocity, thus minimizing the transit time through the channel. A Green's function calculation based on ballistic transport in short CNTs shows that ON/OFF ratios of 10^6 can be achieved, and that the nanotube channel can be as short as 5 nm before tunneling leads to unacceptable leakage currents.[22]

In very recent studies [23] (see also the discussion on n-type and ambipolar CNTFETs), we have found that the Schottky barriers (SB) that form at the source (drain)−nanotube junctions can play a very important role in the switching process. When these barriers dominate the behavior of CNTFETs, switching involves the modulation of the SBs, that is, of the contact resistance, by the gate field. However, phenomenologically, the behavior of an SB−CNTFET should be very similar to that of a conventional transistor; i.e., as a function of increasing V_{GS}, one still observes a linear increase in I_{DS}, followed by a saturation regime.[23] However, the physical processes responsible for this behavior are different and it is no longer appropriate to extract a mobility from the slope of the $I_{DS} - V_{GS}$ curves.

Fabrication and Performance of Carbon Nanotube Field-Effect Transistors

The first demonstrations that nanotubes can be used as field effect transistors (CNTFETs) appeared in 1998.[24,21] The structure of these early CNTFETs was very simple. A SWCNT was positioned on top to bridge two noble metal electrodes, which acted as the source and drain (See Figure 3). The electrodes were fabricated on top of a SiO_2 film grown on a silicon wafer, and the wafer itself was used as the gate ("back-gate") electrode. These CNTFETs behaved as p-type FETs; i.e., the dominant carriers were holes, and the ON/OFF current ratio was $\approx 10^5$. Although functional, the devices had a high parasitic contact resistance (≥ 1 MΩ), low drive currents, and a low transconductance (10^{-9} A/V = nS).

To reduce the contact resistance and improve the characteristics of the CNTFETs, we adapted a different fabrication scheme in which the semiconductor SWNTs (s-CNTFETs) are dispersed on an oxidized Si wafer, and the source and drain electrodes made of metals that are compatible with silicon technology, such as Ti or Co, are

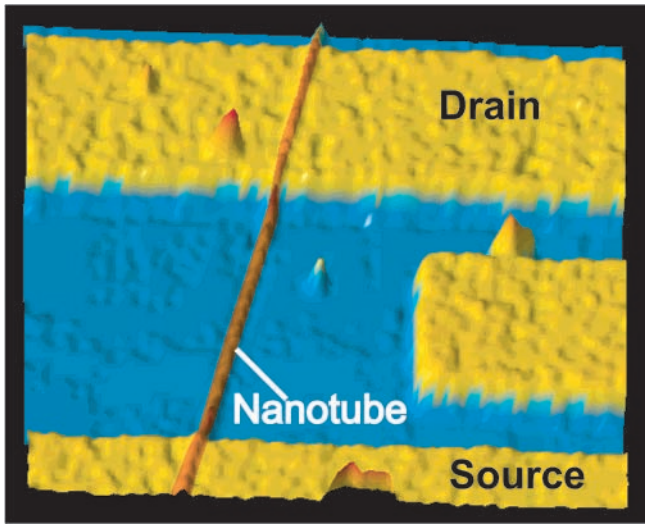

FIGURE 3. Atomic force microscope (AFM) image of a back-gated carbon nanotube FET (CNTFET). A single-walled CNT forms the FET channel connecting gold source and grain electrodes. The heavily doped wafer acts as the gate.

fabricated on top of the s-SWCNTs.[25,26] Subsequent thermal annealing leads to stronger coupling between the metal and the nanotube and a reduction of the contact resistance.

Figure 4A,B shows the output and transfer characteristics of a CNTFET employing Co electrodes.[26] From the $I_d - V_g$ curves, we see that the transistor is ON for negative gate bias that is the transistor is p-type. From the logarithmic scale in Figure 4B, we see that the ON/OFF current ratio is quite high, $\sim 10^6$. This "end-bonded" CNTFET configuration has a significantly reduced contact resistance, $\sim$30 kΩ, and a transconductance $g_m = 3.4 \times 10^{-7}$ A/V (0.34 μS), which is $\sim$200 times higher than that of side-bonded [21] CNTFETs.

All of the above-discussed devices were back-gated with very thick gate insulators ($t_{ox} = 150$ nm of SiO_2). As was already indicated, we should be able to improve their performance by reducing the insulator thickness, thus increasing C_G (eq 1). Furthermore, it is highly desirable to gate each CNTFET independently by its own gate so that complex integrated circuits can be built. In the top of Figure 5, we show a schematic representation of a top-gated CNTFET, and in the bottom, the output characteristics of such a device with Ti source, drain and gate electrodes and a 15-nm SiO_2 gate insulator film.[27] Such a CNTFET can also be switched by the bottom gate (wafer), and the resulting characteristics can be compared with those of the device under top-gate operation. A much superior performance is obtained with top gating. First, the threshold voltage of the top-gated CNTFET is much lower, -0.5 V, than under bottom-gated operation, -12 V. Similarly, the drive current is much higher under top gating. Most importantly, the transconductance under top-gate operation is very high, $g_m = 3.35$ μS/nanotube.

Since the objective of nanotube electronics is to be competitive with silicon electronics, it is important to compare their relative performances, despite the fact that the CNTFETs are still far from being optimized. To do this,

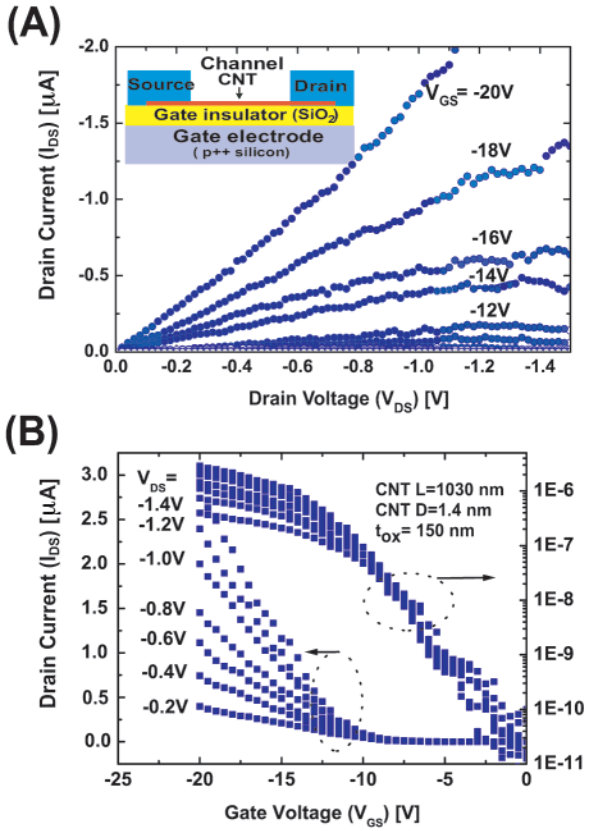

FIGURE 4. (A) Output and (B) transfer electrical characteristics of a CNTFET with cobalt electrodes at room temperature.[26]

we express all the quantities per unit width (μm) of the device, as is the practice in microelectronics (A different way of scaling where a raft of nanotubes is assumed with the appropriate spacing and overall width is discussed in ref 26). The diameter of the s-CNTs used is $\sim$1.4 nm.[28] We find that the ON current of a good top-gated CNTFET is 2100 μA/μm at $V_{ds} = V_{gs} - V_t = 1.3$ V.[27] To our knowledge, the highest reported current drive in a Si p-CMOS under the same bias conditions is 650 μA/μm, achieved in a 50-nm gate length, model CMOS transistor.[29] The transconductance of the CNTFET is $g_m = 2300$ μS/μm. This value is to be compared with a $g_m = 650$ μS/μm for the same Si p-CMOS device.[29]

From the above and other considerations, it is clear that CNTFETs, even in this early stage of development, can outperform corresponding Si devices. Further refinements, such as the reduction of the gate insulator thickness and the use of high dielectric constant gate insulators, are straightforward. Furthermore, the recent insights on the role of Schottky barriers in the switching of CNTFETs once incorporated into a modified design will allow additional improvements of their performance.

Ambipolar and n-Type Carbon Nanotube Transistors

In Figure 6, we show the electrical characteristics obtained when a CNTFET with Ti electrodes was passivated with a film of SiO_2 and subsequently annealed in an inert gas or in a vacuum at $T > 700$ °C. This heat treatment converts

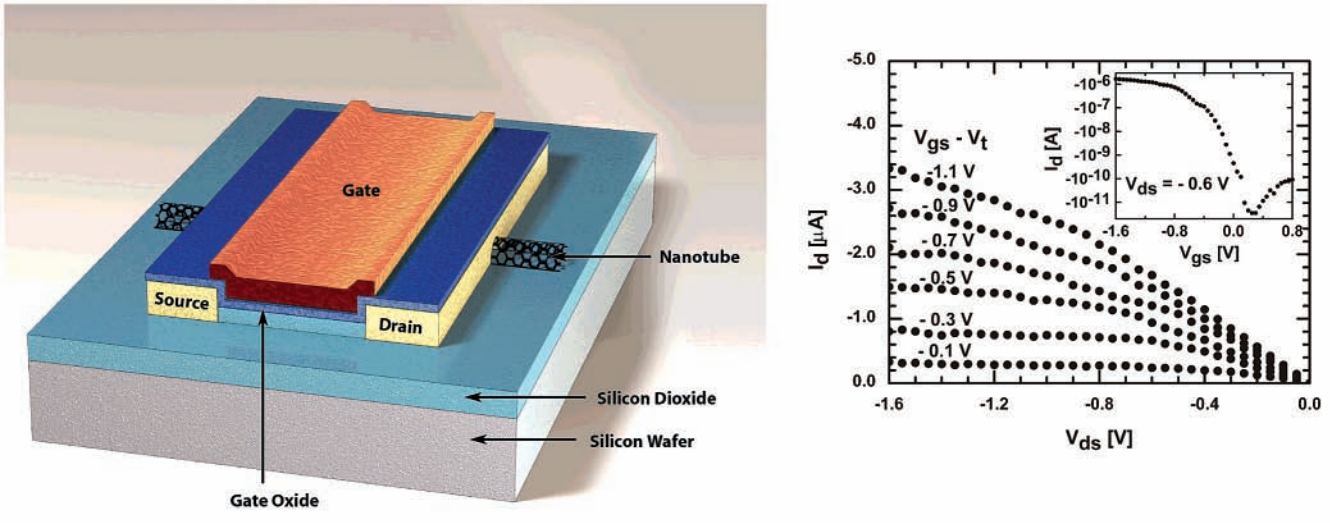

FIGURE 5. (Left) Schematic representation of a top-gated CNTFET. (Right) Room-temperature output electrical characteristics of a 300-nm-long, top-gated CNTFET with a t_{ox} of 15 nm.[27]

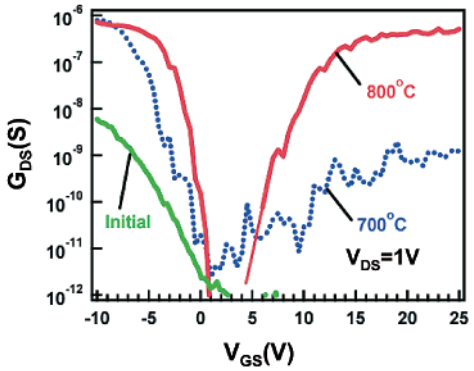

FIGURE 6. Transfer characteristics of an 800-nm-long CNTFET covered with a 10-nm SiO_2 film. The dotted−dashed line shows the characteristics of the device before annealing. The dotted line is obtained after carbide formation and subsequent annealing at 700 °C for 30 s, and the full line is obtained after another anneal at 800 °C for 30 s.[25]

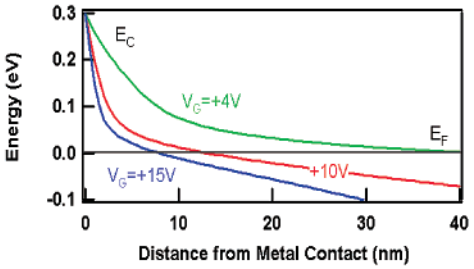

FIGURE 7. Calculation showing the modulation of the 0.3 eV Schottky barrier at a metal/s-CNT (d = 1.4 nm) junction by the gate field.[30]

the contacts to titanium carbide,[25] and the device develops unusual electrical characteristics. Specifically, it passes a strong current at both negative and positive values of V_{GS}; that is, one can get conduction by either holes or electrons in the same device; such a device is called *ambipolar*.

It is well-known that the charge transfer that takes place at the junctions between metals and semiconductors leads to the formation of energy barriers called Schottky barriers.[17] By measuring the electron and hole currents of the ambipolar device as a function of temperature, we can obtain the effective activation barriers for electrons and holes. In this way, very small activation barriers, ∼13 meV for electrons and ∼15 meV for holes, are obtained.[25] These roughly symmetrical barriers suggest that at the junction, the Fermi level lies close to the middle of the s-CNT band gap. (The band gap of ∼1.4 nm s-CNTs is ∼0.6 eV). Now at Si−metal interfaces, the sum of the Schottky barriers for electrons and holes should equal the value of the band gap. In the ambipolar CNTFET, however, the barriers are ∼20 times smaller than $E_g/2$ = 300 meV. The reason for this behavior can be traced to the 1D character of the CNT and the gate field enhancement induced by the needlelike shape of the carbide contacts.[16] Our findings suggest that the actual heights of the Schottky barriers, Φ_0, are larger, but they are thin so that tunneling through the effective barriers dominates the carrier injection process. Furthermore, these barriers can be effectively modulated by the gate field. This is clearly seen in the results of theoretical modeling [30] (see Figure 7).

In computer logic, complementary circuits composed of both n- and p-type FETs have a performance that is far superior to that of the older "ratio logic" circuits based on combinations of resistors and transistors of one type. Thus, to develop nanotube complementary logic circuits, we need to find a way of preparing both types of CNTFETs. However, when CNTFETs are made from as-grown CNTs, without any further processing, the resulting transistors are invariably p-type. A number of explanations have been proposed for this behavior, such as doping by unknown dopants during the synthesis and handling of the CNTs, or charge transfer from high work-function metal electrodes..[24] One way to generate n-type CNTFETs is by doping p-type devices using electron donors, such as alkali metals.[31] Figure 8 shows $I_{DS} - V_{GS}$ curves as a function of increasing exposure to potassium atoms of an initially p-type CNTFET. It is clear that at high exposures, an n-type CNTFET is produced. There is, however, an even easier way to perform the p- to n- transformation.[32,33] As

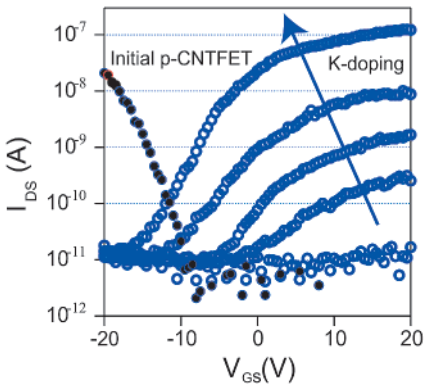

FIGURE 8. Variation of the characteristics of an initially p-type CNTFET as a function of increasing exposure to a potassium atom flux.

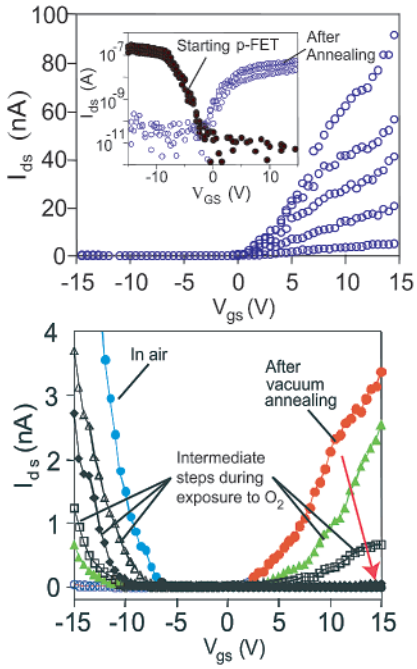

FIGURE 9. (A) Transfer characteristics of an n-type CNTFET obtained by annealing a p-type device in a vacuum at 700K for 10 min. Inset: Comparison of the effect of the gate before and after the annealing. (B) Effect of oxygen exposure on the n-CNFFET. The gradual conversion of the n-CNTFET back into a p-CNTFET is shown as a function of O_2 exposure (2 min at pressures from 10^{-4} to 10^{-1} Torr).[33]

Figure 9A shows, by simply heating a p-CNTFET under vacuum, a process that desorbs any adsorbed gases such as O_2, the CNTFET is converted to an n-type device. Furthermore, this transformation is reversible. In Figure 9B an n-type CNTFET, produced by vacuum annealing, is exposed to increasing amounts of O_2. A reduction of the n-character and a simultaneous buildup of the p-character is observed, the system evolving through a sequence of intermediate stages exemplifying ambipolar character. The above experiments strongly suggest that interaction with O_2 is responsible for the p-character of CNTFETs in air.

An effect of O_2 on the electrical properties of CNTs was first reported by Collins et al..[34] Specifically, an increase in the electrical resistance and changes in the STM spectra of CNTs upon evacuation were observed, and theoretical studies[35] suggested that the effect of O_2 is to dope the CNTs with holes. There are, however, a number of observations that do not seem to support this scenario. First, if oxygen were the dopant responsible for the p-characteristics, then after oxygen desorption, i.e., removal of the dopant, the CNT should become intrinsic, not n-type, as observed. In addition, by comparing the intermediate stages of K-doping in Figure 8 with the intermediate stages of O_2 exposure in Figure 9B, we see significant differences. Increased K-doping leads to threshold-voltage shifts, and enhanced current at $V_{GS} = 0$. No such shifts or nonzero current at $V_{GS} = 0$ are observed in the case of O_2 exposure. These [32,33] observations suggest two distinct mechanisms for the p- to n- conversion induced by potassium and oxygen.

The dominance of one carrier in a semiconductor may be the result of doping, a bulk effect, or it may be determined by Schottky barriers at the metal−semiconductor junction. These barriers may allow the injection of only one type of carrier, electron or hole, and are sensitive to the electrostatic effects and charge transfer by foreign species adsorbed at the junctions. On the basis of the above observations and other findings, we proposed that, although oxygen may indeed lead to some doping of the bulk of the CNT, the observed electrical behavior is dominated by its effect on the contact barriers.[33] In air or oxygen, the Fermi level is extrinsically pinned near the valence band maximum, and this pinning is responsible for the p-character of air-exposed CNTFETs. The outgassing of the device changes the band-bending near the contacts, and the position of the Fermi level within the band-gap changes as a function of the amount of oxygen present at the contacts. This model is illustrated in Figure 10, which gives a qualitative picture of the bending of the bands of a p-type and an ambipolar CNTFET near the contacts.

Returning to the formation of the ambipolar device (Figure 6), we note that the ambipolar behavior was observed only when the device was passivated by a film of SiO_2 before the thermal annealing. At the high annealing temperature, O_2 can diffuse through the oxide and desorb. Upon cooling, however, the SiO_2 film protects the device from oxygen.

Carbon Nanotube Transistor Arrays

A major impediment to the large-scale fabrication of CNTFETs is the fact that the current synthetic schemes for SWCNTs generate mixtures of metallic (m) and semiconducting (s) nanotubes. These tubes tend to adhere to each other, forming “ropes” or “bundles”.[28] No good methods exist for the preparation of only m- or s-nanotubes by selective synthesis or postsynthesis separation. If CNTFETs were to be fabricated from such a rope, the metallic tubes in the rope would sort out the device, as shown in Figure 11. Recently, however, we developed the technique of “constructive destruction” [36] that allows the m-CNTs in a rope to be selectively destroyed, leaving the s-CNTs intact.

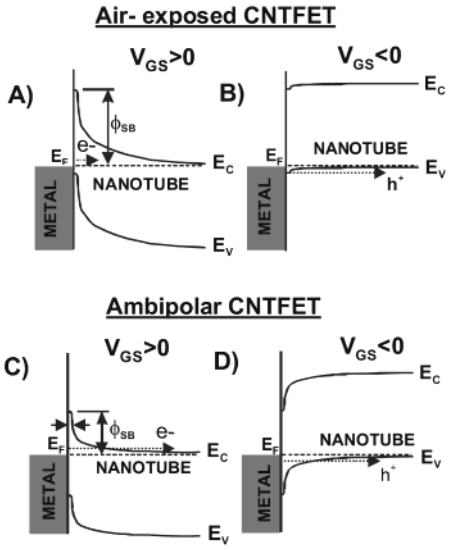

FIGURE 10. Qualitative potential energy curves showing the bending of a semiconducting nanotube valence and conduction bands near the nanotube/metal interface. Curves A and B show the band-bending in air (p-CNTFET), whereas curves C and D depict the behavior of an ambipolar CNTFET.[25,33]

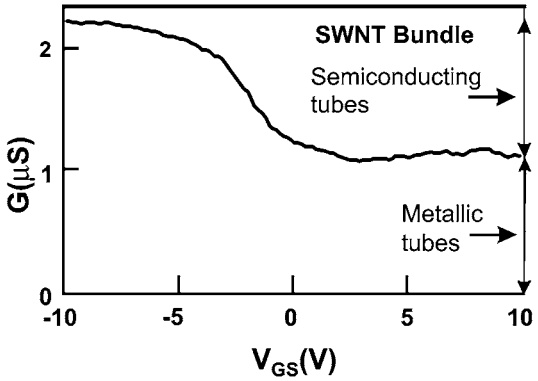

FIGURE 11. The conductance (G) of a single-walled nanotube bundle containing both semiconducting nanotubes as a function of gate voltage.

As we discussed earlier, CNTs can carry enormous current densities at low electron energies. At higher energies, however, optical phonon excitation is possible.[19] This leads to current saturation and the deposition of large amounts of energy, which eventually destroys the CNT structure.[36,37] To apply this method to remove m-tubes from bundles, we first deposit the bundles on an oxidized Si wafer, then we fabricate on them an array of source-drain and side-gate electrodes. By applying an appropriate voltage bias to the gate, the s-CNTs can be depleted of their carriers. Then when a sufficiently high source-drain bias V_{ds} is applied, the generated current passes only through the m-CNTs, leading to their destruction while leaving the s-CNTs essentially intact.[36] (see Figure 12) In this way, arrays of CNTFETs can be generated.

Carbon Nanotube Integrated Circuits: Logic Gates

Having developed ways to fabricate both p- and n-CNTFETs, the natural next step is to produce integrated

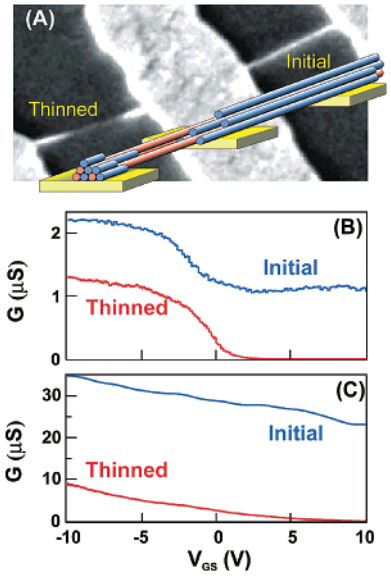

FIGURE 12. (A) AFM image of a single-walled nanotube bundle after breakdown of its metallic tubes. (B) and (C) The conductance of two nanotube bundles before and after breakdown. The semiconducting nanotubes were depleted by applying a V_{GS} of +10 V.[36]

circuits out of them. Of particular interest are logic gates that form the basis of computer logic. The optimal way of forming such circuits involves the use of complementary transistors, that is, both p- and n-type. Complementary circuits have many advantages over logic circuits based on resistor/single type FET, the so-called "ratio logic" technology. Specifically, they consume less power, can have higher gain, are immune to fluctuations in the characteristics of the FET, and are easier to implement in integrated circuits. As a result, complementary logic technology has dominated silicon technology.

A simple example of a logic gate is a voltage inverter or "NOT" gate. As the name implies, this circuit reverses the sign of an input voltage, or by associating, for example, negative voltage with a logical "0", it coverts it to a logical "1" and vice versa. This gate is one of three fundamental circuits from which all other logic gates can be derived.

Figure 13 shows the fabrication of an inverter based on two CNTFETs.[32] It shows the I_{DS} vs V_G curves of two originally p-type CNTFETs, one with the nanotube protected by a film of PMMA and the other unprotected (13A). After they were both annealed in a vacuum, they converted to n-type (13B). Upon reexposure to oxygen, the unprotected CNTFET converts to a p-type device, while the one protected by PMMA remains n-type (13C). By wiring the two CNFETs as shown in Figure 13A, we produce an *intermolecular* voltage inverter.[32] This inverter works exactly the same way as an ordinary CMOS inverter. The input voltage is applied simultaneously to the gates of the two complementary CNFETs. The p-CNFET is polarized by a positive voltage, the n-FET by a negative voltage, and a common contact is used as the intermolecular inverter's output. A positive input voltage turns the n-CNFET ON (the p-CNFET being OFF), resulting in the transmission of the negative voltage to the output. A negative input, on the other hand, turns the p-CNFET ON,

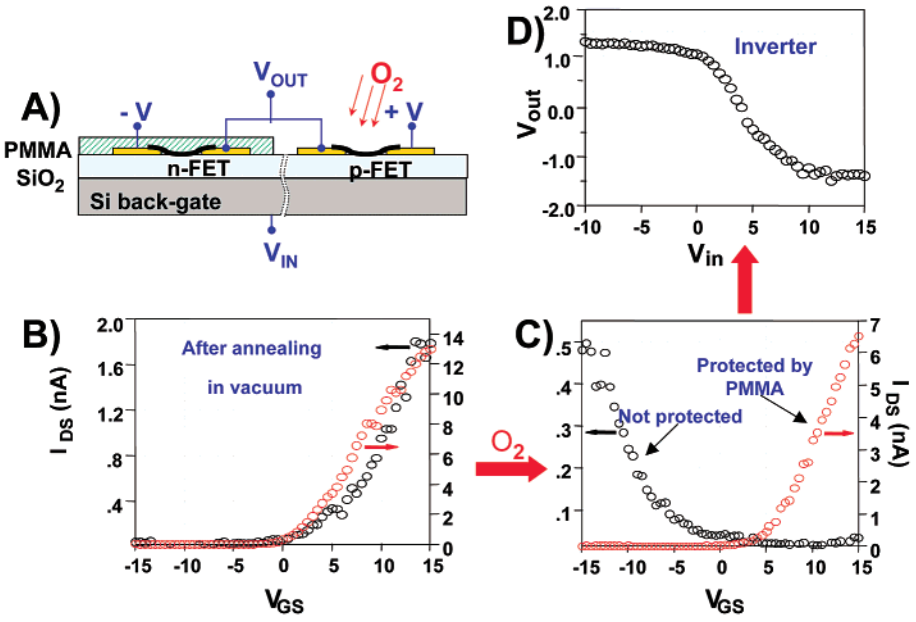

FIGURE 13. Fabrication of a voltage inverter ("NOT" gate) using two CNTFETs. (A) Schematic representation of the circuit. (B) After vacuum annealing, both initially p-type CNTFETs become n-type. (C) Both n-CNTFETs are exposed to oxygen (10^{-3} Torr of O_2 for 3 min). The unprotected n-CNTFET (black circles) converts back to p-type, but the protected CNTFET (red circles) remains n-type. (D) Characteristics of the resulting intermolecular inverter ($V = \pm 1.5$ V).[32]

producing a positive output. The observed transfer curve $V_{OUT}(V_{IN})$ is, indeed, characteristic of a "NOT" logic gate; V_{OUT}, changes from negative to positive (or from "0" to "1") when the input voltage changes from positive to negative values.

In the case of CNTFETs, the ultimate level of integration involves building an integrated circuit along the length of the same nanotube molecule, that is, producing an *intramolecular* logic circuit. An implementation of this concept is shown in Figure 14A.[32] It shows an atomic force microscope (AFM) image of a small SWCNT bundle deposited on top of three gold electrodes. The entire device is first covered by PMMA, and then a window is opened using e-beam lithography. Potassium is used to dope part of the nanotube through this window to produce an n-CNTFET,[38] while the part protected by the PMMA film remains p-type. For convenience, a common back gate is used. The transfer curves shown in Figure 14B demonstrate that this circuit indeed behaves as an intramolecular NOT logic gate.

To use a logical gate as part of a more complicated computing system, a gain higher than one is required. The intramolecular inverter shown in Figure 14A, despite the back-gated configuration with a very large gate oxide thickness (~150 nm), has a gain of ~1.6; therefore, its output can be used to drive another gate or a more complicated logic circuit. The gain of the gate depends on the characteristics of the individual CNTFETs. As we saw above, individually top-gated CNTFETs with thin gate insulator films have the required improved performance and, in addition, allow the fabrication of complex integrated circuits. Another example of nanotube logic gates, however, utilizing resistor/p-CNTFET ratio logic were demonstrated recently.[39] Going beyond nanotubes, Lieber

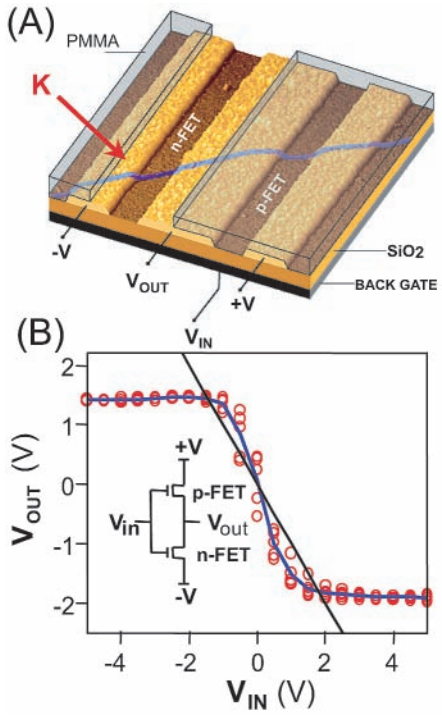

FIGURE 14. (A) AFM image showing the design of an intramolecular logic gate. A SWCNT is positioned over the gold electrodes to produce two p-type CNTFETs in series. The device is covered by a resist (PMMA), and a window is opened by *e*-beam lithography to expose part of the nanotube. Potassium deposited through this window produces an n-CNTFET, but the other CNTFET remains p-type. (B) Electrical characteristics of the intramolecular voltage inverter. Open circles are raw data for five individual measurements on the same device ($V = \pm 2$ V). The solid line is the average of these five measurements. The straight line corresponds to an output/input gain of one. Inset: Schematic representation of the inverter.[32]

and co-workers have provided beautiful examples of logic gates constructed using silicon nanowires.[40]

Conclusions and the Future

Carbon nanotube-based field effect transistors have excellent operating characteristics that are as good as or better than state-of-the-art silicon devices. The performance of CNTFETs is far from being optimized, and significant improvements are expected soon. CNTs do not have interface states that need passivation, as in the case of the $Si-SiO_2$ interface, which makes it easier to integrate the CNTs with high ϵ-dielectrics. Furthermore, the high conductivity and exceptional stability of metallic nanotubes makes them excellent candidates for future use in interconnects. Although CNTs are currently one of the most promising materials for molecular electronics, many challenges remain before they can become a successful technology. Most of these challenges involve the synthesis, separation, and self-assembly of CNTs. Local catalytic growth[41] and alignment of CNTs by electric fields or microfluidic techniques have already been demonstrated in the laboratory. New types of synthetic approaches that operate at lower temperatures may be more selective. Selectivity could also be obtained by the use of seeded growth. The first phase of the work on nanotubes was dominated by physical studies of their electronic structure and properties. Recent advances in the solubilization of CNTs have made possible the application of liquid-phase chemistry and chemical spectroscopy in the modification and characterization of the structure of CNTs. Appropriate functionalization of the nanotubes can help achieve the self-assembly of CNT circuits. To a great extent, the future of nanotube electronics is now in the hands of the chemists.

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